

## PATENT CLAIMS

1. A memory and/or data processing device having at least two stacked layers that overlap each other partially or completely, wherein said layers are supported by a substrate or alternatively forming a sandwiched self-supporting structure of such stacked layers, and wherein at least two layers in the stack comprise memory and/or processing circuitry that connects electrically to memory and/or processing circuitry in at least one other layer and/or said substrate, characterized in that
- 10 said layers are arranged in relation to each other such that contiguous layers form a staggered structure on at least one edge of said device, the edge of at least two layers in said structure forming a set of angular or sloped steps where each step has a height corresponding to the thickness of each layer, and that
- 15 at least one electrical edge conductor is provided passing over the edge of one layer and down one step at a time enabling the connection to an electrical conductor in any of the layers following in the staggered structure.
2. A memory and/or data processing device according to claim 1, characterized in that said
- 20 at least one electrical conductor is provided passing over the edge of said staggered structure and connecting electrically to in-layer conductors in two or more and up to a plurality of contiguous layers, negotiating one step at a time.
3. A memory and/or data processing device according to claim 2, characterized in that
- 25 said in-layer conductors form electrical connections between electrical conductors negotiating the step up to the contiguous layer above and/or down to the contiguous layer below.
4. A method for manufacturing a memory and/or data processing device having at least two stacked layers that overlap each other partially or completely, wherein said layers are supported by a substrate or alternatively forming a sandwiched self-supporting structure of such stacked layers, and wherein at least two layers in the stack comprise memory and/or processing circuitry that connects electrically to memory and/or processing circuitry in
- 30 at least one other layer and/or substrate, and wherein the method is
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characterized by  
comprising steps for adding said layers successively, one layer at a time such  
that the layers form a staggered structure and for providing one or more  
layers with at least one electrical contacting pad for linking to one or more  
5 interlayer edge connectors.

5. A method according to claim 4,  
characterized by providing said layers on a supporting substrate, and forming  
said staggered structure as a step pyramid.

10 6. A method according to claim 4,  
characterized by  
providing said layers on a supporting substrate and forming said staggered  
structure as an inverted pyramid, each of said layers connecting to said  
substrate via said electrical edge connectors negotiating a single step.

15 7. A method according to claim 4,  
characterized by  
forming said edge connectors in a process selected among one of the  
following, viz. lithography, dry etching, inkjet printing, silk screen printing,  
soft lithography, electrolysis, electrostatic deposition, or in situ conversion.

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